**ICX445AQA**

**Description**

The ICX445AQA is a diagonal 6.0mm (Type 1/3) interline CCD solid-state image sensor with a square pixel array and 1.25M effective pixels.

Progressive scan enables all pixel signals to be output separately within 1/22.5 second.

The sensitivity and smear are improved drastically through the adoption of EXview HAD CCD technology.

**Features**

- Supports following modes
  - All-pixel scan mode (15 frame/s, 12.5 frame/s, 22.5 frame/s: **MAX**) 
  - Center cut-out mode (30 frame/s, 25 frame/s) 
- Horizontal drive frequency: 36.0MHz, 29.0MHz 
- R, G, B primary color filters on chip 
- High resolution, high sensitivity, low dark current, low smear 
- Excellent anti-blooming characteristics 
- No voltage adjustments (Reset gate and substrate bias need no adjustment.) 
- 24-pin high precision plastic package (Dual-surface reference available)

**Package**

24-pin DIP (Plastic)

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**EXview HAD CCD™**

* EXview HAD CCD is a trademark of Sony Corporation. The EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation Diode) sensor.

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Element Structure

- Interline CCD image sensor
- Image size
  Diagonal 6.0mm (Type 1/3)
- Total number of pixels
  1348 (H) × 976 (V) approx. 1.32M pixels
- Number of effective pixels
  1296 (H) × 966 (V) approx. 1.25M pixels
- Number of active pixels
  1280 (H) × 960 (V) approx. 1.23M pixels
- Chip size
  6.26mm (H) × 5.01mm (V)
- Unit cell size
  3.75μm (H) × 3.75μm (V)
- Optical black
  Horizontal (H) direction: Front 12 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits
  Horizontal (H) direction: Front 4 pixels
  Vertical (V) direction: Front 2 pixels
- Substrate material
  Silicon

Optical Black Position

(Top View)
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Block Diagram and Pin Configuration

Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>Vϕ2B</td>
<td>Vertical register transfer clock</td>
<td>13</td>
<td>VOUT</td>
<td>Signal output</td>
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<tr>
<td>2</td>
<td>Vϕ2A</td>
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<td>GND</td>
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<td>Vϕ3B</td>
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<td>16</td>
<td>ϕRG</td>
<td>Reset gate clock</td>
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<tr>
<td>5</td>
<td>Vϕ1B</td>
<td>Vertical register transfer clock</td>
<td>17</td>
<td>LHϕ1</td>
<td>Horizontal register final stage transfer clock</td>
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<td>18</td>
<td>Hϕ2A</td>
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<td>7</td>
<td>Vϕ4B</td>
<td>Vertical register transfer clock</td>
<td>19</td>
<td>Hϕ1A</td>
<td>Horizontal register transfer clock</td>
</tr>
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<td>8</td>
<td>Vϕ4A</td>
<td>Vertical register transfer clock</td>
<td>20</td>
<td>Hϕ1B</td>
<td>Horizontal register transfer clock</td>
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<tr>
<td>9</td>
<td>VϕST</td>
<td>Horizontal addition control clock</td>
<td>21</td>
<td>Hϕ2B</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>10</td>
<td>VϕHLD</td>
<td>Horizontal addition control clock</td>
<td>22</td>
<td>ϕSUB</td>
<td>Substrate clock</td>
</tr>
<tr>
<td>11</td>
<td>VL</td>
<td>Protective transistor bias</td>
<td>23</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
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<td>24</td>
<td>VDD</td>
<td>Supply voltage</td>
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Absolute Maximum Ratings

<table>
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<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
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<tbody>
<tr>
<td>Against $\phi$SUB</td>
<td>$V_{DD}, V_{OUT}, \phi_{RG} - \phi_{SUB}$</td>
<td>$-39$</td>
<td>$+12$</td>
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<td>V</td>
<td></td>
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<tr>
<td></td>
<td>$\phi_{2A}, \phi_{2B}, \phi_{3A}, \phi_{3B} - \phi_{SUB}$</td>
<td>$-46$</td>
<td>$+17$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\phi_{1A}, \phi_{1B}, \phi_{4A}, \phi_{4B}, \phi_{ST}, \phi_{HLD}, VL - \phi_{SUB}$</td>
<td>$-46$</td>
<td>$+0.3$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$H_{\phi1A}, H_{\phi1B}, H_{\phi2A}, H_{\phi2B}, LH_{\phi1}, GND - \phi_{SUB}$</td>
<td>$-39$</td>
<td>$+0.3$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Against GND</td>
<td>$V_{DD}, V_{OUT}, \phi_{RG} - GND$</td>
<td>$-0.3$</td>
<td>$+20$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\phi_{1A}, \phi_{1B}, \phi_{2A}, \phi_{2B}, \phi_{3A}, \phi_{3B}, \phi_{4A}, \phi_{4B}, \phi_{ST}, \phi_{HLD} - GND$</td>
<td>$-9.0$</td>
<td>$+17$</td>
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<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$H_{\phi1A}, H_{\phi1B}, H_{\phi2A}, H_{\phi2B}, LH_{\phi1} - GND$</td>
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<td>$+4.2$</td>
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<td>V</td>
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<tr>
<td>Against VL</td>
<td>$\phi_{2A}, \phi_{2B}, \phi_{3A}, \phi_{3B} - VL$</td>
<td>$-0.3$</td>
<td>$+25$</td>
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<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$\phi_{1A}, \phi_{1B}, \phi_{4A}, \phi_{4B}, \phi_{ST}, \phi_{HLD}, H_{\phi1A}, H_{\phi1B}, H_{\phi2A}, H_{\phi2B}, LH_{\phi1}, GND - VL$</td>
<td>$-0.3$</td>
<td>$+13$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Between input clock pins</td>
<td>Potential difference between vertical clock input pins</td>
<td>$to +13$</td>
<td></td>
<td></td>
<td>V</td>
<td>$^*$1</td>
</tr>
<tr>
<td></td>
<td>$H_{\phi1A}, H_{\phi1B} - H_{\phi2A}, H_{\phi2B}$</td>
<td>$-5$</td>
<td>$+5$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$H_{\phi1A}, H_{\phi1B}, H_{\phi2A}, H_{\phi2B} - \phi_{4B}, \phi_{HLD}$</td>
<td>$-13$</td>
<td>$+13$</td>
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<td>V</td>
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<td>Storage temperature</td>
<td>$-30$</td>
<td>$+80$</td>
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<td>°C</td>
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<td>Operating temperature</td>
<td>$-10$</td>
<td>$+60$</td>
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<td>°C</td>
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</table>

$^*$1 $+25$V (Max.) is guaranteed when clock width $< 10 \mu$s, clock duty factor $< 0.1\%$.

Bias Conditions

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<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
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<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
<td></td>
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<tr>
<td>Protective transistor bias</td>
<td>$V_{L}$</td>
<td></td>
<td></td>
<td>$^*$1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Substrate clock</td>
<td>$\phi_{SUB}$</td>
<td></td>
<td></td>
<td>$^*$2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>$\phi_{RG}$</td>
<td></td>
<td></td>
<td>$^*$2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^*$1 $V_{L}$ setting is the $V_{VL}$ voltage of the vertical clock waveform, or the same voltage as the $V_{L}$ power supply for the $V$ driver should be used.

$^*$2 Do not apply a DC bias to the substrate clock and the reset gate clock pin, because a DC bias is generated internally.

DC Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
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<tr>
<td>Supply current</td>
<td>$I_{DD}$</td>
<td>10.0</td>
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<td>mA</td>
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## Clock Voltage Conditions

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<th>Item</th>
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<th>Min.</th>
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<th>Max.</th>
<th>Unit</th>
<th>Waveform diagram</th>
<th>Remarks</th>
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<tr>
<td>Readout clock voltage</td>
<td>$V_{VT}$</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
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<tr>
<td>Vertical transfer clock voltage</td>
<td>$V_{VH2}, V_{VH3}$</td>
<td>0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
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<tr>
<td>Horizontal transfer clock voltage</td>
<td>$V_{VH1}, V_{VH4}, V_{VHSTR}, V_{VHL}$</td>
<td>0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset gate clock voltage</td>
<td>$V_{VRG}$</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
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<tr>
<td>Substrate clock voltage</td>
<td>$V_{SUB}$</td>
<td>22.5</td>
<td>23.5</td>
<td>24.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Remarks</td>
<td>$V_{VH} = (V_{VH2} + V_{VH3})/2$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
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<td>Remarks</td>
<td>$V_{VL} = (V_{VL1} + V_{VL4})/2$</td>
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<td>V</td>
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<tr>
<td>Remarks</td>
<td>$V_{VH} = V_{VHL} - V_{VLL}$</td>
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<td></td>
<td>V</td>
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<tr>
<td>Remarks</td>
<td>$n = 1$ to $4$</td>
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<td></td>
<td></td>
<td>V</td>
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<tr>
<td>Item</td>
<td>Symbol</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td>Unit</td>
<td>Remarks</td>
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<td>Capacitance between vertical</td>
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<td>1200</td>
<td>pF</td>
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<td>transfer clock and GND</td>
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<td>2700</td>
<td>pF</td>
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<td></td>
<td>$C\Phi V3A, C\Phi V3B$</td>
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<td>pF</td>
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<td>$C\Phi V4A, C\Phi V4B$</td>
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<td>pF</td>
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<td>$C\Phi VS, C\Phi VHLD$</td>
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<td>pF</td>
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<tr>
<td>Capacitance between vertical</td>
<td>$C\Phi V1A V1B, C\Phi V2A V2B$</td>
<td>220</td>
<td>pF</td>
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<td>transfer clocks</td>
<td>$C\Phi V1A V4B, C\Phi V1B V4A$</td>
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<td>pF</td>
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<td></td>
<td>$C\Phi V2A V3A, C\Phi V2B V3B$</td>
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<td>pF</td>
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<td></td>
<td>$C\Phi V3A V4A, C\Phi V3B V4B$</td>
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<td>pF</td>
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<td>$C\Phi V3A VS, C\Phi V4A VHLD$</td>
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<td>pF</td>
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<td>$C\Phi V4A VS, C\Phi VS VHLD$</td>
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<td>$C\Phi H2$</td>
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<td>$C\Phi RG$</td>
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<td>Capacitance between reset gate</td>
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<td>clock and GND</td>
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<tr>
<td>Vertical transfer clock series</td>
<td>$R\Phi V1A, R\Phi V1B$,</td>
<td>39</td>
<td>Ω</td>
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<td>resistor</td>
<td>$R\Phi V4A, R\Phi V4B$,</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>$R\Phi VS, R\Phi VHLD$</td>
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<td>Vertical transfer clock ground</td>
<td>$RGND$</td>
<td>15</td>
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<td>resistor</td>
<td>$R\Phi H1A, R\Phi H1B$</td>
<td>18</td>
<td>Ω</td>
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<td>Horizontal transfer clock series</td>
<td>$R\Phi H2A, R\Phi H2B$</td>
<td>16</td>
<td>Ω</td>
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<tr>
<td>resistor</td>
<td>$R\Phi SUB$</td>
<td>300</td>
<td>kΩ</td>
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</table>
Vertical transfer clock equivalent circuit

Horizontal transfer clock equivalent circuit
Drive Clock Waveform Conditions

1. Readout clock waveform

2. Vertical transfer clock waveform

\[ V_{\phi_1A}, V_{\phi_1B}, V_{\phi_ST} \]

\[ V_{\phi_2A}, V_{\phi_2B} \]

\[ V_{\phi_3A}, V_{\phi_3B} \]

\[ V_{\phi_4A}, V_{\phi_4B}, V_{\phi_{HLD}} \]

\[ V_{\phi} = (V_{\phi_2} + V_{\phi_3})/2 \]

\[ V_{\phi} = (V_{\phi_1} + V_{\phi_4})/2 \]

\[ V_{\phi} = V_{\phi_{HH}} - V_{\phi_{LN}} (n = 1 to 4) \]
3. Horizontal transfer clock waveform

Cross-point voltage for the Hφ1A, Hφ1B and LHφ1 rising side of the horizontal transfer clocks Hφ1A, Hφ1B, LHφ1 and Hφ2A, Hφ2B waveforms is $V_{CR}$.

The overlap period for $t_{wh}$ and $t_{wl}$ of horizontal transfer clocks Hφ1A, Hφ1B, LHφ1 and Hφ2A, Hφ2B is “two”.

4. Reset gate clock waveform

$V_{RG}$ is the minimum value during the interval $t_{wh}$, then:

$V_{φRG} = V_{RG} - V_{RGL}$

Negative overshoot level during the falling edge of $RG$ is $V_{RGLm}$.

5. Substrate clock waveform

$V_{sub}$ is a bias generated internally.

$V_{φM} = \frac{1}{2} (V_{RGH} + V_{RGLL})$

Assuming $V_{RGH}$ is the minimum value during the interval $t_{wh}$, then:

$V_{φRG} = V_{RGH} - V_{RG}$

$V_{φM}$ is the maximum value and $V_{RGH}$ is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of $RG$.

In addition, $V_{RG}$ is the average value of $V_{RGH}$ and $V_{RGLL}$.

$V_{RG} = \frac{1}{2} (V_{RGH} + V_{RGLL})$
### Clock Switching Characteristics

(Horizontal drive frequency: 36.0MHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>twh</th>
<th>twl</th>
<th>tr</th>
<th>tf</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout clock</td>
<td>Vt</td>
<td>1.52</td>
<td>1.72</td>
<td>0.5</td>
<td>0.5</td>
<td>μs</td>
<td>During readout</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using CXD3400N</td>
</tr>
<tr>
<td>Horizontal transfer clock</td>
<td>LHϕ1, Hϕ1A, Hϕ1B</td>
<td>8</td>
<td>9</td>
<td>8</td>
<td>9</td>
<td>ns</td>
<td>When driving at 3.6V during imaging, tf ≥ tr – 2ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hϕ2A, Hϕ2B</td>
<td>8</td>
<td>9</td>
<td>8</td>
<td>9</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>ϕRG</td>
<td>4</td>
<td>5.5</td>
<td>17</td>
<td>2</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Substrate clock</td>
<td>ϕSUB</td>
<td>0.9</td>
<td>1.8</td>
<td>0.25</td>
<td>0.25</td>
<td>μs</td>
<td>When draining charge</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>two</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Horizontal transfer clock</td>
<td>LHϕ1, Hϕ1A, Hϕ1B, Hϕ2A, Hϕ2B</td>
<td>8</td>
<td>9</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

![Spectral Sensitivity Graph](image-url)
## Image Sensor Characteristics (Center cut-out drive, 30 frame/s)

*(Ta = 25°C)*

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Measurement method</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>G sensitivity</td>
<td>Sg</td>
<td>300</td>
<td>380</td>
<td></td>
<td>mV</td>
<td>1/30s accumulation</td>
<td></td>
</tr>
<tr>
<td>Sensitivity ratio</td>
<td>R Rr</td>
<td>0.55</td>
<td>0.81</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B Rb</td>
<td>0.23</td>
<td>0.49</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Saturation signal</td>
<td>Ysat</td>
<td>350</td>
<td></td>
<td></td>
<td>mV</td>
<td>2</td>
<td>Ta = 60°C</td>
</tr>
<tr>
<td>Smear</td>
<td>Sm</td>
<td></td>
<td></td>
<td>-104</td>
<td>dB</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Video signal shading</td>
<td>SHg</td>
<td>20</td>
<td>25</td>
<td>85</td>
<td>%</td>
<td>4</td>
<td>Zone 0 and I</td>
</tr>
<tr>
<td>Uniformity between</td>
<td>ΔSrg</td>
<td>8</td>
<td>25</td>
<td>8</td>
<td>%</td>
<td>5</td>
<td>Zone 0 to II'</td>
</tr>
<tr>
<td>video signal channels</td>
<td>ΔSbg</td>
<td>8</td>
<td>25</td>
<td>8</td>
<td>%</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Dark signal</td>
<td>Vdt</td>
<td>2</td>
<td></td>
<td>2</td>
<td>mV</td>
<td>6</td>
<td>Ta = 60°C, 1/30s accumulation</td>
</tr>
<tr>
<td>Dark signal shading</td>
<td>ΔVdt</td>
<td>1</td>
<td></td>
<td>1</td>
<td>mV</td>
<td>7</td>
<td>Ta = 60°C, 1/30s accumulation*1</td>
</tr>
<tr>
<td>Line crawl R</td>
<td>Lcr</td>
<td>3.8</td>
<td>3.8</td>
<td>8</td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Line crawl B</td>
<td>Lcb</td>
<td>3.8</td>
<td>3.8</td>
<td>8</td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Lag</td>
<td>Lag</td>
<td>0.5</td>
<td>0.5</td>
<td>9</td>
<td>%</td>
<td>9</td>
<td></td>
</tr>
</tbody>
</table>

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

### Zone Definition of Video Signal Shading

![Zone Definition of Video Signal Shading](image)

### Measurement System

![Measurement System](image)

Note) Adjust the amplifier gain so that the gain between [*A*] and [*B*], and between [*A*] and [*C*] equals 1.
Image Sensor Characteristics Measurement Method

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

Color coding of this image sensor & Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure above (Bayer array). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

The R signal and Gr signal lines and Gb signal and B signal lines are output successively.
Definition of standard imaging conditions

◆ Standard imaging condition I:
  Use a pattern box (luminance: 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
  Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G sensitivity, sensitivity ratio
   Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (VGr, VGb, VR and VB) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.
   \[
   V_G = \frac{(V_{Gr} + V_{Gb})}{2} \\
   S_g = V_G \times \frac{(100/30)}{\text{[mV]}} \\
   R_r = \frac{V_R}{V_G} \\
   R_b = \frac{V_B}{V_G}
   \]

2. Saturation signal
   Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
   Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.
   \[
   S_m = 20 \times \log \left\{ V_{Sm} \div \left( \frac{(Gra + Gba + Ra + Ba)}{4} \right) \times \left( \frac{1}{500} \right) \times \left( \frac{1}{10} \right) \right\} \text{[dB]}
   \]

4. Video signal shading
   Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum value (Gmax) and minimum value (Gmin) of the Gr signal and substitute the values into the following formula.
   \[
   S_{Hg} = \frac{(G_{max} - G_{min})}{150 \times 100} \%
   \]

5. Uniformity between video signal channels
   After the measurement item 4, measure the maximum (Rmax) and minimum (Rmin) values of the R signal and the maximum (Bmax) and minimum (Bmin) values of the B signal, and substitute the values into the following formula.
   \[
   \Delta S_{Rg} = \frac{(R_{max} - R_{min})}{150 \times 100} \%
   \Delta S_{Bg} = \frac{(B_{max} - B_{min})}{150 \times 100} \%
   \]

6. Dark signal
   Measure the average value of the signal output (Vdt) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.
7. Dark signal shading
   After the measurement item 6, measure the maximum (Vdmax) and minimum (Vdmin) values of the dark signal output and substitute the values into the following formula.

   \[ \Delta V_{dt} = V_{d\text{max}} - V_{d\text{min}} \text{ [mV]} \]

8. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (\(\Delta G_r, \Delta G_g, \Delta G_b\)) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

   \[ L_{ci} = (\Delta G_i/G_i) \times 100 \% \quad (i = r, g, b) \]

9. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   \[ \text{Lag} = (V_{\text{lag}}/150) \times 100 \% \]
Connecting a 1 MΩ grounding resistor to Pin 22 (φSUB) is not necessary.

Connect a constant current source with low collector output capacitance (Cob value (current value 2 to 6 mA) to Pin 13 (VOUT).

When performing oscillation, connect a resistor and/or a capacitor to the base. Select the optimum value from approximately 2 to 6 mA for the constant current value and the rear-end emitter current value in consideration of the load capacitance.

The Vs value can be adjusted in the range of 0.0 to 5.0 V ± 5%. Raising the Vs electric potential reduces heat generated at the constant current source and buffer connected to the VOUT pin. Be careful because the value of the resistor connected to the constant current source and buffer transistor varies according to the value of Vs.

\[
\begin{align*}
(Vb - Vs) / ((15 - Vb) / 10) & [k \Omega] \\
(Vb - Vs - 0.8) / 3 & [k \Omega] \\
(Vb - Vs - 0.8) / 4.5 & [k \Omega]
\end{align*}
\]

When emitter current is 3 mA.

When constant current is 4.5 mA.
Drive Timing Chart

All-pixel Scan Mode (15 frame/s) Vertical Direction

The TGVD in this chart is noted at 1456H (1H: 1650 clocks). (1 clock = 6.0MHz)
All-pixel Scan Mode (12.5 frame/s) Vertical Direction

The TGVD in this chart is noted at 1450H (1H: 1600 clocks). (1 clock = 29.0MHz)
All-pixel Scan Mode (22.5 frame/s) Vertical Direction

The TGVD in this chart is noted at 1001H (1H: 1600 clocks). (1 clock = 36.0MHz)
Center Cut-out Mode (30 frame/s) Vertical Direction

The TGVD in this chart is noted at 750H (1H: 1598 clocks) + 1H (2700 clocks: fractional adjustment line). (1 clock = 36.0MHz)
Center Cut-out Mode (25 frame/s) Vertical Direction

- TGVD
- TGHD
- Sub
- V1
- V2A
- V2B
- V3A
- V3B
- V4
- VHA
- VST (VSTR)
- CCD OUT
- PBLK
- CPD
- CPDM

Fractional adjustment line

Frame shift

High-speed sweep

$\alpha (156 \text{ steps})$

$10H + \alpha (130 \text{ steps})$

$6H + \alpha (150 \text{ steps})$

$\theta_{\text{fractional adjustment}} = 744H (1H: 1556 \text{ clocks}) + 1H (2336 \text{ clocks})$ (fractional adjustment line).

1 clock = 29.0 MHz
All-pixel Scan Mode (15 frame/s): from the falling edge of the 60H TGHD to 144 clocks (end)

All-pixel scan mode (12.5 frame/s): from the falling edge of the 52H TGHD to 120 clocks (end)

Drive frequency: 36.0MHz (15 frame/s)
29.0MHz (12.5 frame/s)

* Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD and synchronize the falling edge of SUB with the first rising edge of VHLD counting from (a).

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD. The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.
Center cut-out Mode (30 frame/s)
Center cut-out mode (25 frame/s)

Drive frequency: 36.0MHz (30 frame/s)
29.0MHz (25 frame/s)

Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD and
synchronize the falling edge of SUB with the first rising edge of VHLD counting from (a).

The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.
The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD. The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz. When there is no number in parentheses, the count is the same for both 36.0 MHz and 29.0 MHz.
All-pixel Scan Mode (15 frame/s, 12.5 frame/s, 22.5 frame/s)/ Center Cut-out Mode (30 frame/s, 25 frame/s)

Horizontal Direction Readout Block [C]

The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.

The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.
Center Cut-out Mode (30 frame/s)

Center Cut-out Mode (25 frame/s)

Horizontal Direction Frame Shift Block [D]

Drive frequency: 36.0MHz (30 frame/s)
29.0MHz (25 frame/s)

- SUB pulse generation is prohibited during the frame shift period.
- The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
  The numbers on the upper level are for 36.0 MHz, and the numbers in parentheses on the lower are for 29.0 MHz.
Notes On Handling

1. Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling CCD image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the package temperature does not exceed 80°C.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

   ![Diagram](Compressive strength)

   Compressive strength

   50N 50N

   Torsional strength

   ![Diagram](Torsional strength)

   1.2Nm

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
(4) The notch of the package is used for directional index, and that cannot be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
**Package Outline**

(Unit: mm)

1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference. The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B'" is \((H, V) = (8.0, 7.1) \pm 0.075\text{mm}\).
5. The rotation angle of the effective image area relative to \(H\) and \(V\) is \(\pm 1^\circ\).
6. The height from the bottom "C" to the effective image area is 1.41mm \(\pm 0.1\text{mm}\).
7. The height from the top of the cover glass "D" to the effective image area is 1.49mm \(\pm 0.15\text{mm}\).
8. The tilt of the effective image area relative to the bottom "C" is less than 35µm.
9. The tilt of the effective image area relative to the top "D" of the cover glass is less than 50µm.
10. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.

---

**PACKAGE STRUCTURE**

<table>
<thead>
<tr>
<th>Plastic</th>
<th>GOLD PLATING</th>
<th>LEAD MATERIAL</th>
<th>LEAD ALLOY</th>
<th>PACKAGE MASS</th>
<th>DRAWING NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS-A16(E)</td>
<td>42 ALLOY</td>
<td>1.20g</td>
<td>1.0g</td>
<td>AS-A16(E)</td>
<td></td>
</tr>
</tbody>
</table>

---

Sony Corporation